Conductive interconnections through thick Si substrate

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Two key technologies, Optical Excitation Electro-polishing Method (OEEM) and Molten Metal Suctioned Method (MMSM), to form metal filled Through-Holes (THs) from the front to the back of thick Si wafer (~500μm), have been developed. The OEEM is a wet-etching technology that has the capability to produce very high aspect ratio (more than 100) THs in Si substrate. The MMSM is a technique of filling the TH with molten metal in vacuum. The conductive interconnections formed by the both technologies have very good performances of individual insulation (more than 500V dielectric breakdown voltage) and leakage free structure between the front and the back of the substrate. We experimentally made 500THs/cm^2 in a thick Si substrate, each of which has an opening 15μm in the diameter and the aspect ratio of 35. These THs were filled with several different kinds of metal in the trials after the formation of insulation layers. Both technologies can be applied in Si terraces for MOEMS device, Si Optical Bench (SiOB), 3D-stacked IC packaging or other System In Package (SIP) to minimize the size and the cost.

KEYWORDS: optical excitation electropolishing method (OEEM), through-hole electrode, molten metal suctioned method (MMSM), interconnection, silicon optical bench, silicon terrace, 3D stack, IC package, system in package (SIP)

1. Introduction

Forming conductive interconnections through Si substrate is one of the essential technologies for high-density packages, module assemblies and/or system integration. Thinner back grinded wafers are typically used in those applications, such as memory modules. Consequently, Deep-Reactive Ion Etching (DRIE), usually Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE) is adopted, for Si TH forming, Plasma Enhanced-Chemical Vapor Deposition (PE-CVD) for insulator forming and electro or non-electro plating for metal interconnection can be applied thanks to the backside grinding of the Si substrate.

On the other hand, thicker wafers are preferred in Micro Optical Electro-Mechanical System (MOEMS), which isn't allowed to be grinded and/or polished for the backside of the substrate, or in SiOB on which the high heat generating laser diode is mounted. Due to the thick substrate, there are some obstacles to be overcome to form the conductive interconnections through Si.

1.1 Forming TH

DRIE or laser processes are typical techniques to make TH in Si substrate. DRIE is often used in forming MEMS devices, which require complex structures and a high speed-etching rate. However it has limitations in a deep etching as forming a high aspect ratio TH on the ground of the difficulties in supplying of attacking species from the front opening to the bottom of the THs. In addition, the formed shape by DRIE is usually barrel one, which may make troubles in later processes. One of problems in laser forming is wall roughness as it physically breaks Si. Another is the diameter difference between the etching front and the backside and the tact time during a high-density process.

While the OEEM[1,2] is one of alternatives to form a high aspect ratio (more than 100) and a good forthrightness (less than 0.5°), the substrate must be n-type (100) and there are two major problems for practical applications. One is so-called 'side-branch', which is etching profile proceeding to a certain undesirable [010] and [001] directions. The other is 'peripheral effect', which is a phenomenon that THs located at the edge of relatively high-density pattern have much more the 'side-branch'. We have improved the sidewall quality of THs to reduce the depth of the 'side-branch' and the 'peripheral effect' to use the methods in practical applications.

1.2 Metal filling

Electro or non-electroplating are typical techniques to form conductive interconnections in the THs. However, those methods cannot be applied for filling a high aspect ratio TH due to the impossibilities in circulation of the plating solution causing undesirable voids in the metal. The MMSM[3] we have proposed is an excellent technology to fill Si THs with metals,

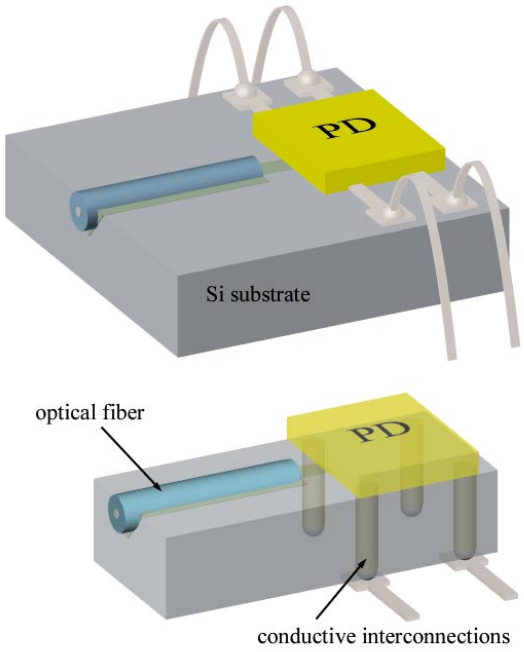

Fig.1 Schematic illustration of SiOB without (above) and with (below) conductive interconnections through thick Si substrate.

of which melting point and vaporization pressure at the melting point are low respectively.

The schematic comparison between the SiOB applied conductive interconnections through Si substrate and an ordinal wire bonding solution is shown in Fig.1. It is apparent that the SiOB using conventional wire bonding occupies a larger device area than the TH solution's. In addition, the fabrication cost with solder bumps connecting to the THs must be lower than wire bonding process's.

This paper describes details of those two key technologies, the OEEM and the MMSM, to form high aspect ratio conductive interconnections through Si substrate, which can be applied for MOEMS, SiOB, 3D-stacked IC packaging and other System In Package (SIP).

2. Forming Process and Discussion

The schematic cross sectional view at each process step of forming metal filled THs in a Si substrate are shown in Fig.2. Si THs are formed by the OEEM. Since the substrate was to be used as Si terraces for an opt-electronic device, we could start the process from a virgin wafer, where no circuits or element was built in advance. Therefore, we could use high temperature thermal oxidation for insulator forming. After the oxidation, the THs are filled with metal by the MMSM.

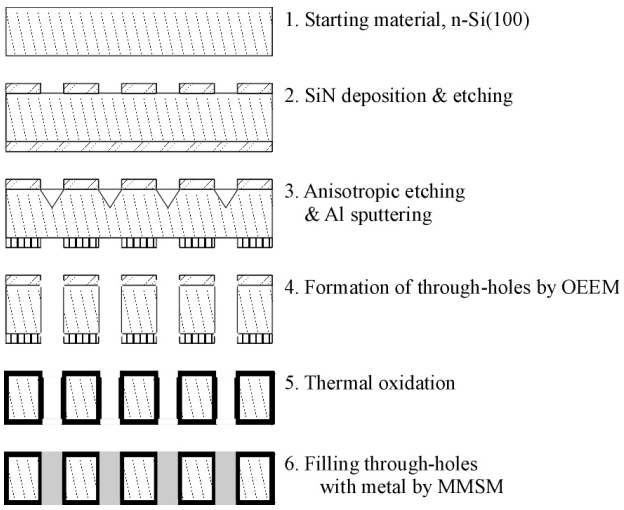

Fig.2 Forming process step for metal filled through-holes.

2.1 TH Forming (OEEM)

The schematic illustration of the OEEM experiment system is shown in Fig.3. The starting material was a n-type, 525μm thickness and double side mirror polished Si wafer, of which direction was (100) grown by the Magnetic Czochralski (MCZ). First, 110nm Si_3N_4 film layer was deposited by LP-CVD. Then, 30nm Cr and 500nm Au films were successively sputtered on Si_3N_4 layer. These metal layers work as protection masks against HF solution. At the same time, they keep uniformity of electrical field between anodic Si wafer and cathode Pt plate in the OEEM system. In order to make initial etch pits, Au/Cr and Si_3N_4 layers are patterned and opened by a typical photolithography and etching on the front surface of the wafer. V-grooves were formed from the opening by anisotropic etching with KOH solution. Typical OEEM conditions are;

- Current density: 6.0mA/cm^2 (DC voltage = 0.5-2.0V)

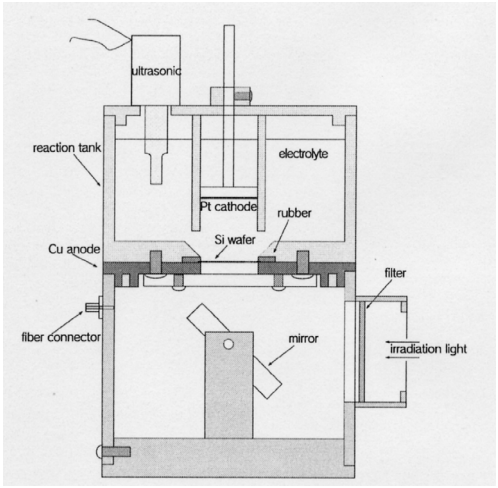

Fig.3 Schematic illustration of OEEM experiment system.

- Light intensity: 5.9mW/cm^2
- Electrolyte: 2.5wt% HF solution
- Surfactant: C_2H_5OH 10%
- Temperature of electrolyte: 50˚C

A mercury lamp was used as the light source to irradiate the backside surface of the wafer, and a band-pass filter (from 370nm to 750nm of wavelength) was placed in the optical path. The followings describe the mechanism of the OEEM. The minority carriers, positive holes in this case, are generated within a depth of approximately 11μm from the bottom surface. They move toward the front surface by the electric field applied to the system. Where the V-groove exists on the front surface of the Si substrate, the electric field concentrates at the peak of the V-groove leading electric charges (positive holes). The chemical reaction as shown below occurs there, and only the certain points where it occurs are etched to form TH.

$$Si + 6HF + \lambda(+) \rightarrow H_2SiF_6 + H_2 + 2H + \lambda(-) \quad (1)$$

The etching rate was around 0.5μm/min. under the optimized conditions for good sidewall morphology of the TH. The cross-sectional views of the THs are shown in Fig.4. The 'side-branches' toward [001] and [010] directions are clearly observed, while the sidewall of [110] direction THs have good morphology.

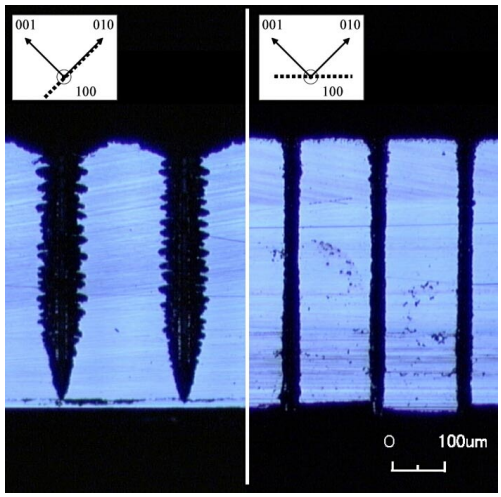

Fig.4 Photograph of cross section of through-holes by OEEM. Broken lines mean cutting planes.

Since the phenomenon had the dependence on crystal orientation, the major mechanism of the 'side-branches' would have relation with the density of the dangling bonds, of which [001] or [010] is higher than [110]'s. The electrolyte based HF solution might attack the Si atoms in the [001] and [010] crystal directions.

Another possible cause of the 'side-branches' was that the generated holes from the backside of Si wafer were pulled up to the [001] or [010] ridges as well as the V-groove peaks because of the electric field concentrations.

In addition, the maximum of the 'side-branches' depth would have relation with the pitch of the THs. Under those our analysis, we have done experiments changing the following conditions to minimize the 'side-branches'.

- Making initial pits by laser process instead of the an isotropic etching, which didn't produce the [001] or [010] ridge
- Changing resistivity of the substrate from 1 to 100Ω.
- Two different pitches of V-groove (80μm and 162.5μm)

Fig. 5 shows the dependence of TH opening diameter and the 'side-branches' depth on substrate resistivity. The diameter was wider according to the increase of the resistivity. This suggests that change of Space Charge Region (SCR), which is defined by the following equation, would dominate the phenomenon.

$$d = [2\varepsilon\varepsilon_0(V_D\text{-}V)/eN_D]^{1/2} \quad (2)$$

As the applied voltage is constant, the SCR around TH expands in accordance with the decrease of the impurity concentrations. Since there are few carriers in SCR, the minority positive holes reached SCR contribute to the etching at the point. SCR in a 100Ω-cm substrate is 10 times wider than a 1Ω-cm substrate's. We speculate that a wider SCR would expand the diameter of the etching opening.

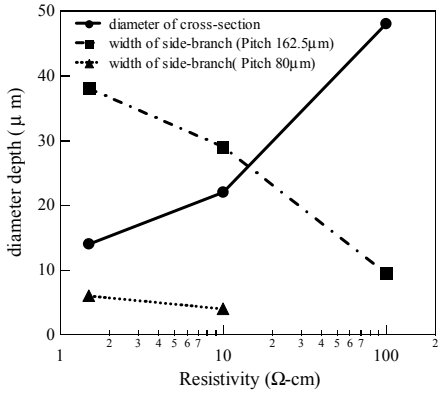

Fig.5 Diameter and 'side-branch' depth as function of Si substrate resistivity.

The depth of the 'side-branches' in a 80-120Ω-cm substrate was 75% less than in a 1-2Ω-cm one. In other words, the 'side-branches' depth becomes shallow according to the increase of the substrate resistivity. In addition, the narrower (80μm) TH pitch improved 13% of the depth compared to the wider (162.5μm) pitch. This means that the narrower pitch restrict supplying holes to each TH, and suppress holes to work at undesired places. On the other hand, non-ridge shaped initial etch pits by laser process wasn't effective to reduce the depth of the 'side-blanches'. This suggests that holes concentration to the ridge of the initial V-groove wasn't the dominant cause of the 'side-branch', therefore the relaxing electric field at V-groove didn't work well to suppress the 'side-branches'.

We finally concluded the reason why the 'side-blanches' were produced was that more dangling bonds of the [001] and [010] was attacked by HF solution and surplus holes compared to [110] direction's.

With regard to the 'peripheral effect', we assumed that excessive holes generated by the backside lighting caused the phenomenon, which usually occurred in the edge THs of relatively high density THs clustering pattern. In order to suppress it, we formed a sputtered Al shade mask at the back surface of the wafer, which has aligned small opening windows corresponding to the front V-groove positions vertically. In the experiment, the light intensity of the backside illumination was set to 49mW/cm^2, which was 50 times larger than that of no shade mask, because total opening area of the mask was a fiftieth of the full opened area. Fig.6 shows how much the backside mask shade improved the 'peripheral effect'. The dependence of the 'peripheral effect' on substrate resistivity and the shade mask are shown in Fig.7. The 'peripheral effect' was minimized to 79% with the shade mask. As we had expected, the shade mask would suppress surplus holes and the 'peripheral effect', however higher substrate resistivity made bigger 'peripheral effect'. We assumed that the worse 'peripheral effect' according to the increase of the substrate resistivity would relate to the SCR, however we need further investigation to be convinced of it.

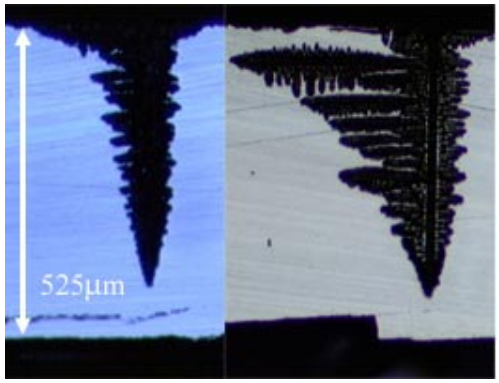

Fig.6 Photograph of cross section of through-holes by OEEM with the backside mask shade (left), the 'peripheral effect' in fully opened backside (right).

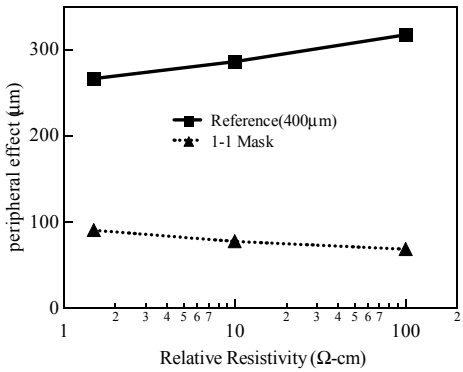

Fig.7 Dependence of the 'peripheral effect' on Si substrate resistivity.

2.2 Insulator forming

After the OEEM process, the protection layers and the backside shade mask, such as Si_3N_4, Al and Au/Cr films were stripped, and then the SiO_2 insulator was formed by thermal

oxidation (1100˚C, 3 hours in steam). The thickness of the SiO_2 film on both the surface of substrate and the sidewall of the THs were 1.2μm, which was measured on cross sectional SEM photograph. If we have to handle IC built in Si substrates, other low temperature insulator forming processes up to 400˚C must be required. The PE-CVD would be the most possible alternative technology, however it is currently difficult for the technology to form reliable and thick enough SiO_2 layers in the high aspect ratio THs.

2.3 Metal filling (MMSM)

The MMSM has a capability to fill the THs with metal using the differential pressure between vacuum and the atmospheric pressure. The selection of the filled metal must be considered as follows;

(1) Low vaporization pressure at the melting point to perform filling operation in vacuum

(2) Low coefficient of thermal expansion to prevent the sucked metal from forming voids due to shrinking during cooling

(3) Low resistivity of metal to make low impedance interconnection

Listed in Table I are several metals that we filled through-holes by MMSM in the experiments.

Table I. Melting points of metals filled through-holes with.

Metal	T_M (˚C)
In	156.4
Sn	231.9
Au-Sn20(wt%)	280.0

The schematic illustration of the MMSM experiment system is shown in Fig.8. In the experiments, the wafer was set in the chamber first, where was evacuated to $5.0x10^{-5}$ torr, and then the melting bath was heated up to 330˚C in case of Sn. THs formed Si was dipped in the bath after the metal melt enough. One minute after the dipping, N_2 gas was introduced to the chamber up to atmospheric pressure (approximately 1bar abs.), and the chamber was pressurized to $2.0kg/cm^2$ by N_2 gas subsequently, then the gate valve was closed. After keeping the pressure for 5 minutes, the valve was released and the sample was taken out from the chamber checking if the remaining metal on the surface had solidified. The excessive metal was removed by wiping during reheating process or wet etching. Fig.9 shows the cross-section views of the Sn buried inside the THs in a thick Si substrate. The THs sized 30μm in the diameter with the aspect ratio of 50 were completely filled without any voids.

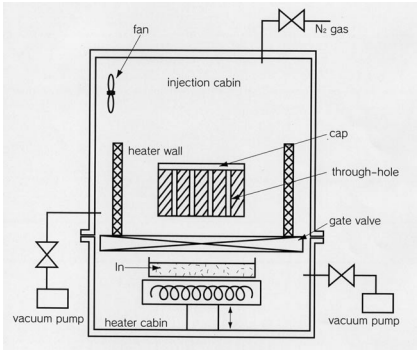

Fig.8 Schematic illustration of MMSM experiment system.

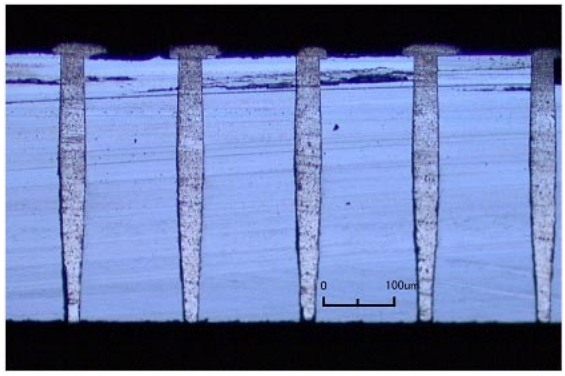

Fig.9 High aspect ratio THs filled with Sn.

2.4 Evaluation

The dielectric breakdown voltage of insulator between the Si substrate and the filled metal was more than 500V, which was large enough for MOEMS applications. And no-leakage between the front and the backside of the Si substrate was confirmed by a Radiflo test.

3. Conclusive Summary

Conductive interconnections through thick Si substrate have been experimentally made using two newly developed technologies. In forming the through-holes, the Optical Excitation Electro-polishing Method (OEEM) has been applied and its 'side-branches' and 'peripheral effect' were improved by controlling substrate resistivity and surplus holes. And it was demonstrated that high aspect ratio THs were filled with a certain metal by the Molten Metal Suctioned Method (MMSM), which had enough individual insulation (more than 500V) and no-leakage between the front and the back of the substrate.

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